ADVANCED MATERIALS

Supporting Information

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An Effective Sneak-Path Solution Based on a Transient-Relaxation Device

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Supplementary Information for

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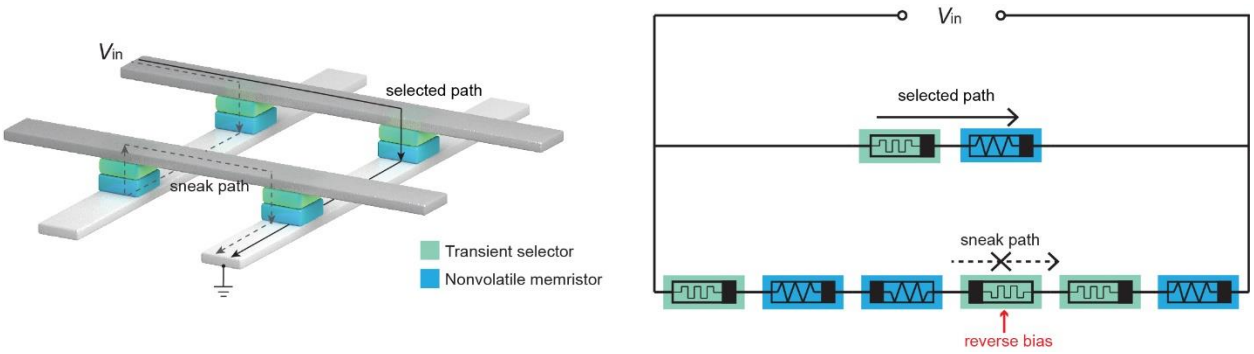
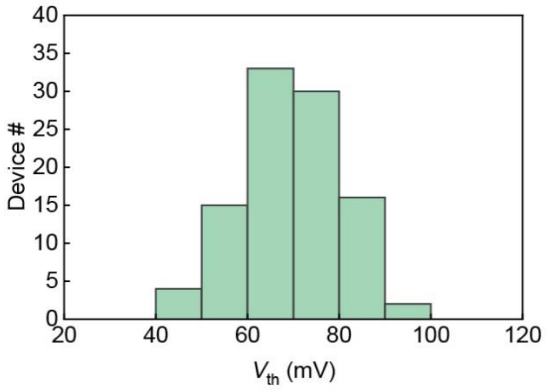
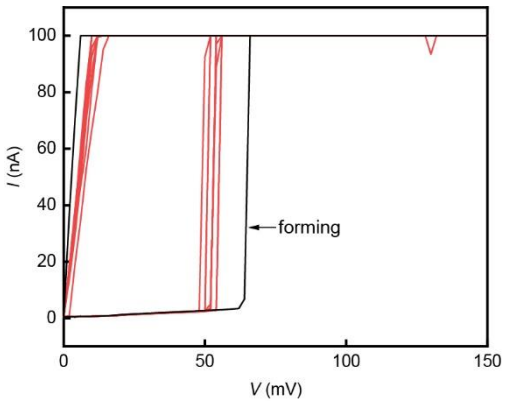


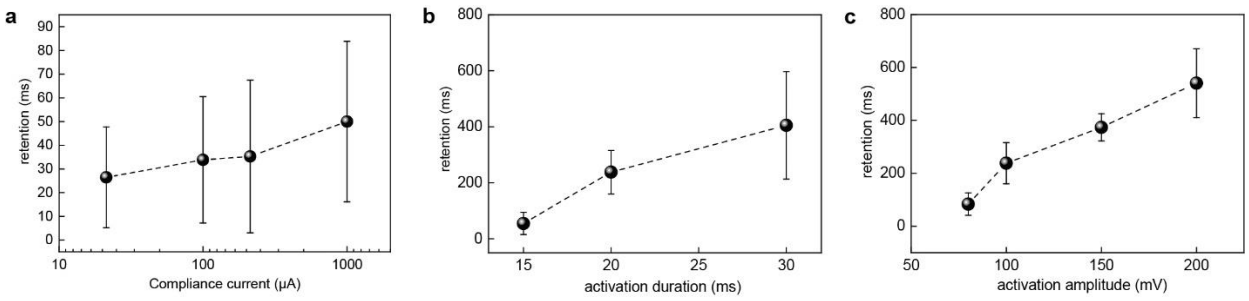
Supplementary Figure S1. Equivalent circuit (left) between the addressed WL (V_{in}) and BL (ground) in a 2×2 array (right). One transient selector (red arrow) in the sneak path is under reverse bias, which then suppresses the current flow (due to the rectifying property in the selector).



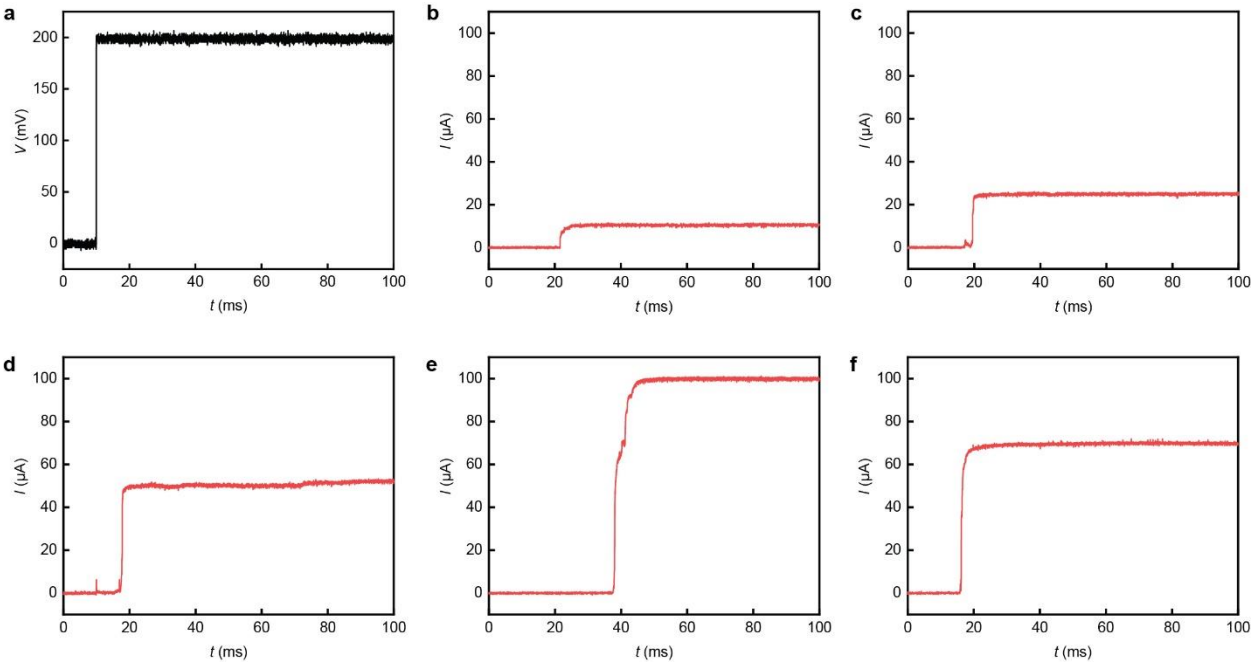
Supplementary Figure S2. Statistical distribution of the average switching voltage (V_{th}) from 100 bio-amplitude volatile memristor (BVMR) devices.



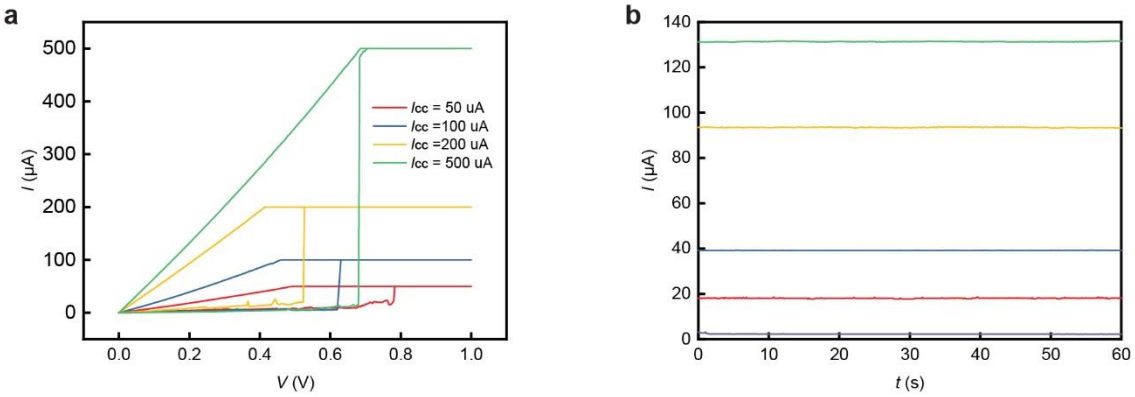
Supplementary Figure S3. A typical forming process in a BVMR device. The black curve represents the first *I*-*V* sweep (0→150 mV →0), followed by 10 continues *I*-*V* sweeps. The average forming voltage in BVMR devices was 83 ± 13 mV (*N*=20), consistent with previous study.[1]



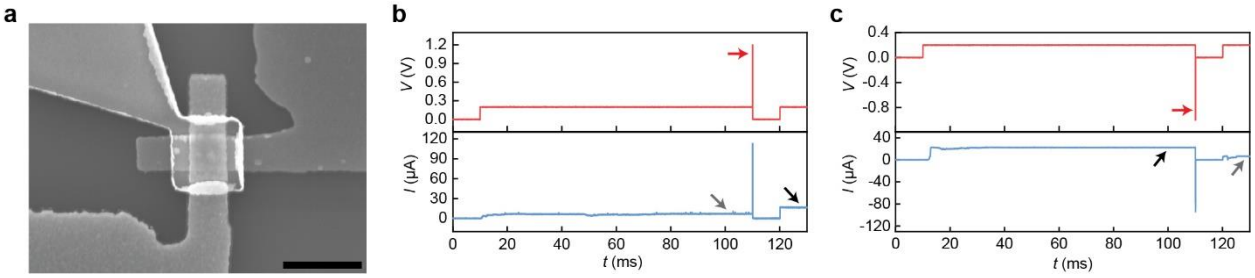
Supplementary Figure S4. Dependence of retention time on various inputs in the BVMR devices. **a**, Average retention with respect to different compliance currents ($N \geq 17$). **b**, Average retention with respect to different activation duration (with fixed amplitude of 100 mV) ($N \geq 10$). Note that a pulse width >10 ms was needed to activate the BVMR. **c**, Average retention with respect to the activation amplitude (with fixed pulse width of 20 ms) ($N \geq 6$).



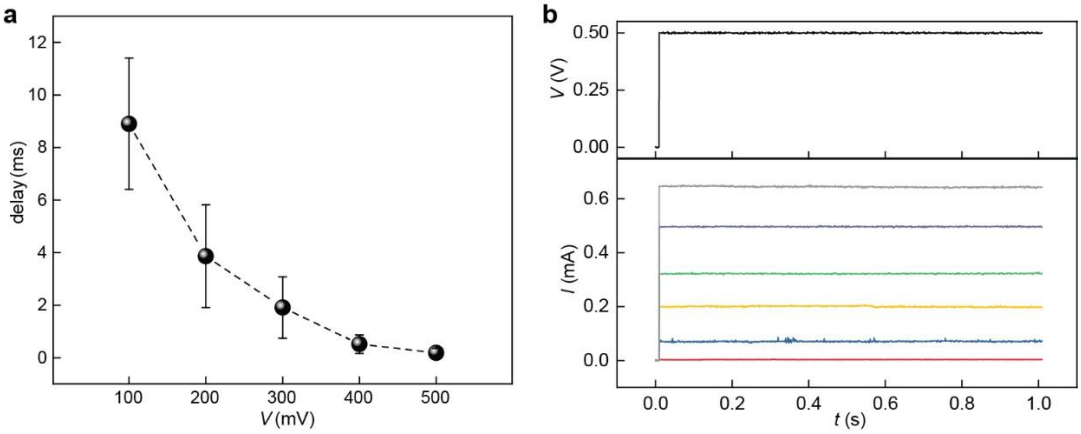
Supplementary Figure S5. Activation of BVMR and reading operation. **a**, A 200-mV pulse is used as the activation voltage. **b-f**, The corresponding activation and simultaneous reading of the conduction in nonvolatile memristors of different programmed states. The average activation time in the BVMR devices without compliance was 8.9 ± 2.5 ms (*N*=40).



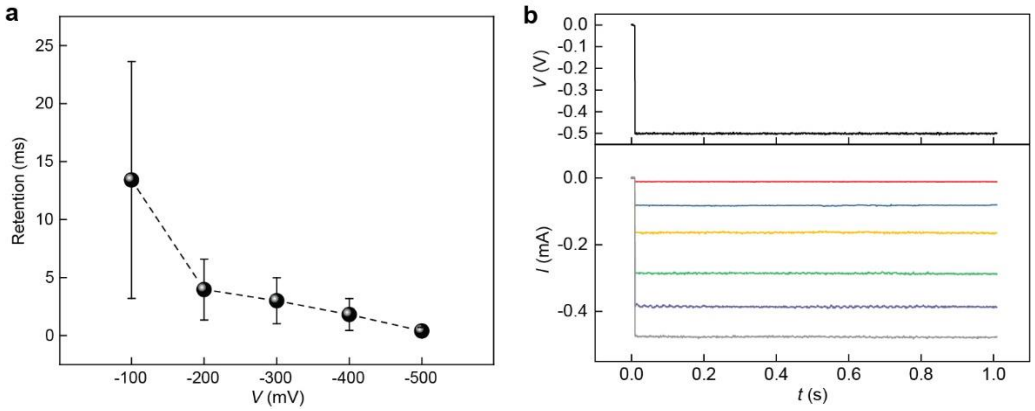
Supplementary Figure S6. Influence of the activation/reading voltage (e.g., 200 mV) on the programmed state in Ta-HfO_2 memristor. **a**, Ta-HfO_2 in the stacking cell was programmed to different conduction states by applying different compliance currents (I_{cc}). **b**, A 200-mV voltage was used to read these different conduction states, which were stable and not altered by the reading voltage.



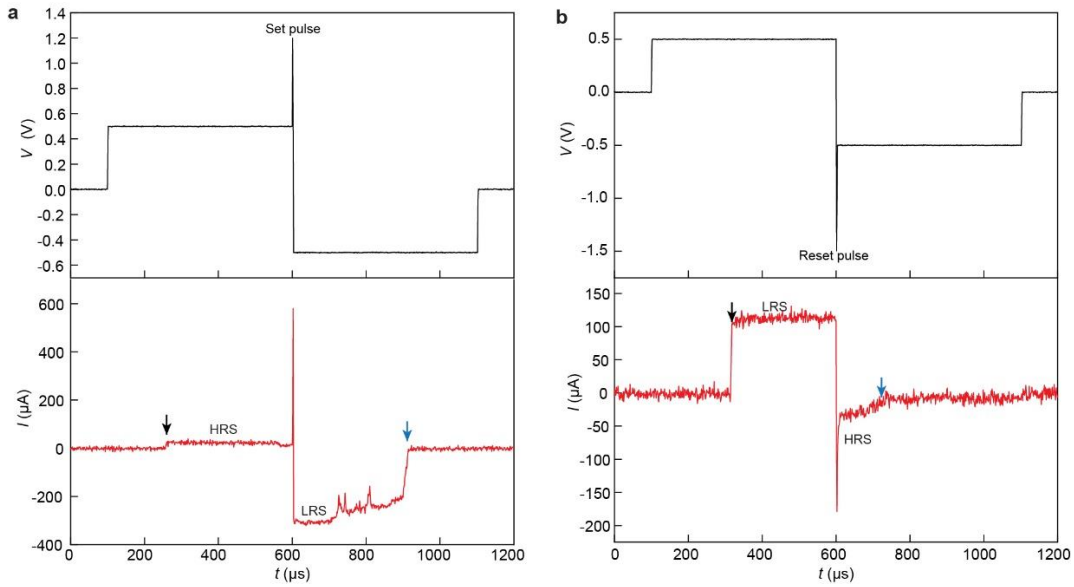
Supplementary Figure S7. Programmability in integrated $1S_{tr}1R$ cell scaled to sub-micrometer size. **a**, Scanning electron microscope (SEM) image of a fabricated cell (~500×500 nm^2) by stacking a BVMR on a Ta-HfO_2 memristor. A middle Pd electrode (top left) was still used. Scale bar, 1 μm. **b**, A SET programming in the cell. A 200-mV pulse (100 ms) first activates the BVMR, indicated by a current raise at *t*~10 ms. A subsequent programming pulse (red arrow, 1.2 V, 100 μs) sets the cell from a high-resistance state (HRS, gray arrow) to a low-resistance state (LRS, black arrow). The success of the SET programming is indicated by the increased current at *t*~120 ms by a 200-mV reading voltage. **c**, A RESET programming in the cell. A 200-mV pulse (100 ms) first activates the BVMR, indicated by a current raise at *t*~17 ms. A subsequent programming pulse (red arrow, -1 V, 100 μs) resets the cell from a LRS (black arrow) to a HRS (gray arrow). The success of the RESET programming is indicated by the decreased current at *t*~120 ms by a 200-mV reading voltage.



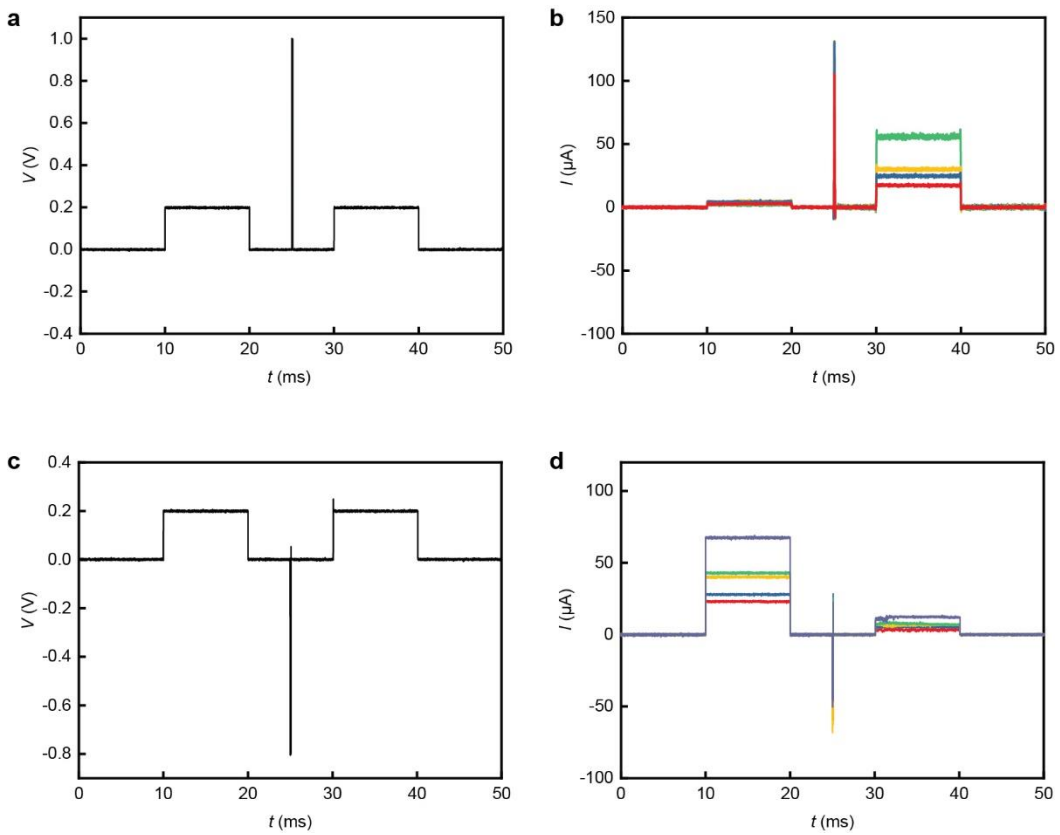
Supplementary Figure S8. Amplitude-dependent delay time in BVMR devices. **a**, Average delay time with respect to the input amplitude ($N \geq 11$). The delay time reduced from 8.9±2.5 ms with a 100-mV input amplitude to 0.19±0.17 ms with a 500-mV input amplitude. **b**, The programmed multiple conductance states in a Ta-HfO_2 memristor (bottom) were not perturbed by the 500-mV voltage amplitude (upper).



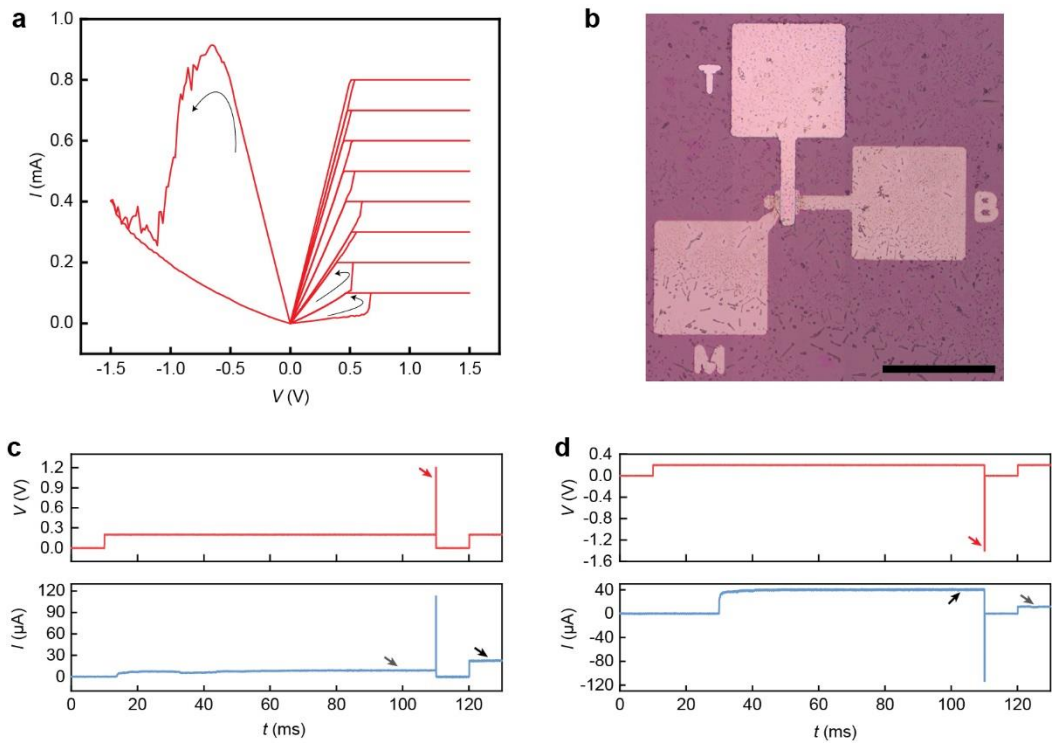
Supplementary Figure S9. Shortening retention in BVMR devices with reverse voltage input. **a**, Average retention time with respect to the amplitude of the reverse voltage ($N \geq 8$). The retention time reduced to 0.40±0.3 ms with the reverse amplitude of -500 mV. **b**, The programmed multiple conductance states in a Ta-HfO_2 memristor (bottom) were not perturbed by the -500-mV reverse voltage (upper).



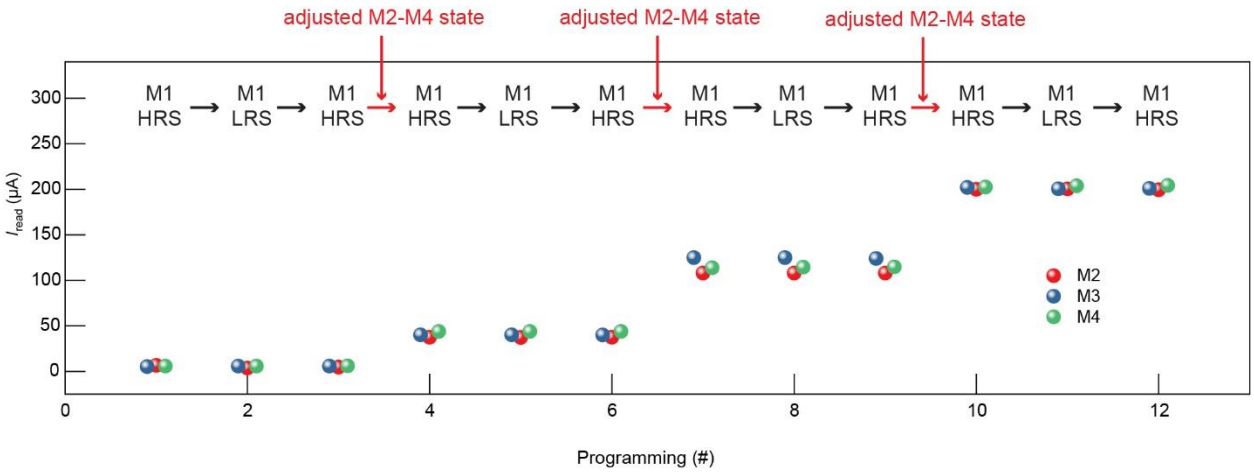
Supplementary Figure S10. Sub-millisecond programming in the integrated BVMR-HfO_2 cell. **a**, A SET programming. A 500-mV voltage was used to activate the BVMR selector in ~0.2 ms (black arrow) and a subsequent SET pulse (1.2 V, 2 μs) was used to program the HfO_2 memristor from a HRS to a LRS. Then a reverse -500-mV pulse was used to deactivate the selector in ~0.3 ms (blue arrow). **b**, A RESET programming. A 500-mV voltage was used to activate the selector in ~0.2 ms (black arrow) and a subsequent RESET pulse (-1.5 V, 2 μs) was used to program the HfO_2 memristor from a LRS to a HRS. Then a reverse -500-mV pulse was used to deactivate the selector in ~0.15 ms (blue arrow).



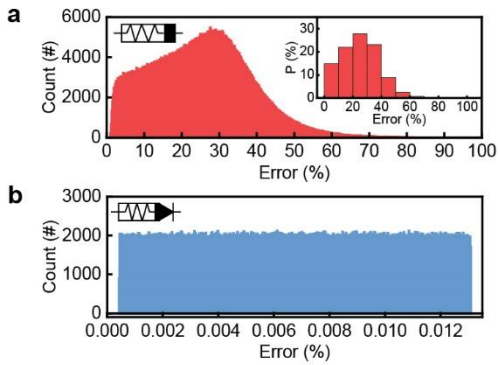
Supplementary Figure S11. SET and RESET programming in the programmable cell constructed from stacking the BVMR on Ta-HfO_2 non-MR. **a**, The input pattern including the 200-mV activation voltage (at t ~ 10-20 ms), SET voltage (at t ~ 25 ms), and a 200-mV reading voltage (at t ~ 30-40 ms). **b**, The corresponding current recorded from the cell with the input in (a). The cell was programmed from a high-resistance state (HRS, t ~ 10-20 ms) to four different low-resistance states (LRS, t ~ 30-40 ms) by imposing different compliance currents (I_{cc}). **c**, Similar input voltage pattern with a 200-mV activation voltage (at t ~ 10-20 ms), RESET voltage (at t ~ 25 ms), and a 200-mV reading voltage (at t ~ 30-40 ms). **d**, The corresponding current recorded from the cell with the input in (c). The cell was programmed from a LRS (t ~ 10-20 ms) to five different HRS (t ~ 30-40 ms) by imposing different compliance currents (I_{cc}).



Supplementary Figure S12. Programmability in $1S_{tr}1R$ cell constructed from stacking a BVMR on a Ta-Ta_2O_5 nonvolatile memristor (non-MR). Device fabrication details can be found in *Methods*. **a**, *IV* sweeps in the Ta/Ta_2O_5/Pt non-MR, showing tunable conductance states at different compliance currents. **b**, Optical image of the integrated $1S_{tr}1R$ cell. Scale bar, 100 μm. **c**, A SET programming in the cell. A 200-mV pulse (100 ms) first activates the BVMR, indicated by a current raise at *t*~17 ms. A subsequent programming pulse (red arrow, 1.2 V, 100 μs) sets the cell from a high-resistance state (HRS, gray arrow) to a low-resistance state (LRS, black arrow). The success of the SET programming is indicated by the increased current at *t*~120 ms by a 200-mV reading voltage. **d**, A RESET programming in the cell. A 200-mV pulse (100 ms) first activates the BVMR, indicated by a current raise at *t*~30 ms. A subsequent programming pulse (red arrow, -1.4 V, 100 μs) resets the cell from a LRS (black arrow) to a HRS (gray arrow). The success of the RESET programming is indicated by the decreased current at *t*~120 ms by a 200-mV reading voltage.

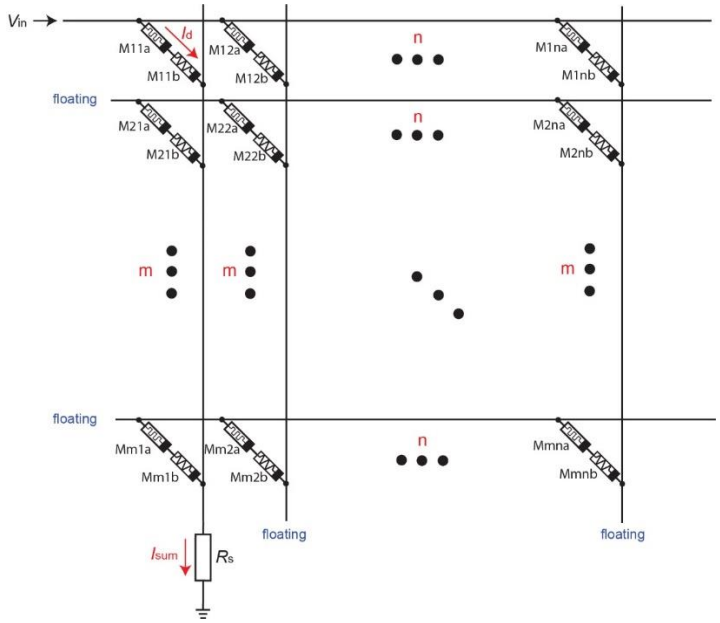


Supplementary Figure S13. Demonstration of repeatedly selected programming. In four programming cycles, in which the selected cell (M1) was programmed from HRS→LRS→HRS (not shown here), the conduction states in the cells (M2-M4) in the sneath path were not altered. To show the robustness, the conduction states of M2-M4 in each cycle were intentionally adjusted to cover the broad range between HRS and LRS.



Supplementary Figure S14. Analysis of the reading error in a 2×2 array. **a**, The probability of the reading error in the array without the BVMR transient selector. The reading error is defined by I_{sneak}/I_{sum}, where I_{sum} and I_{sneak} represent the measured total current and sneak current between the selected WL and BL, respectively. The conduction values of M1-M4 are randomly assigned during the one-million sampling cases. The inset summarizes the corresponding percentile distribution. **b**, The probability of the reading error in the $1S_{tr}1R$ array integrated with the BVMR transient selector. The conduction values of M1-M4 are randomly assigned during the one-million sampling cases.

The calculation of the reading-error distribution was performed by MATLAB 2019b with the following steps: 1) The resistance in M1-M4 was randomly assigned within the range of 1-29 kΩ (corresponding to typical programmable range in Ta-HfO_2 memristors[2]); and experimental values of the On resistance (1 kΩ) and Off resistance (300 MΩ) in the BVMR were used. 2) The reading error was effectively calculated by $err = \frac{R_{M1}}{R_{M1}+R_{M2}+R_{M3}+R_{M4}}$;



Supplementary Figure S15. Sneak-path analysis in general-sized array. The current-based read margin (RM) is defined as[3,4]

$$RM = \frac{I_{LRS\_min} - I_{HRS\_max}}{I_{LRS\_min}},$$

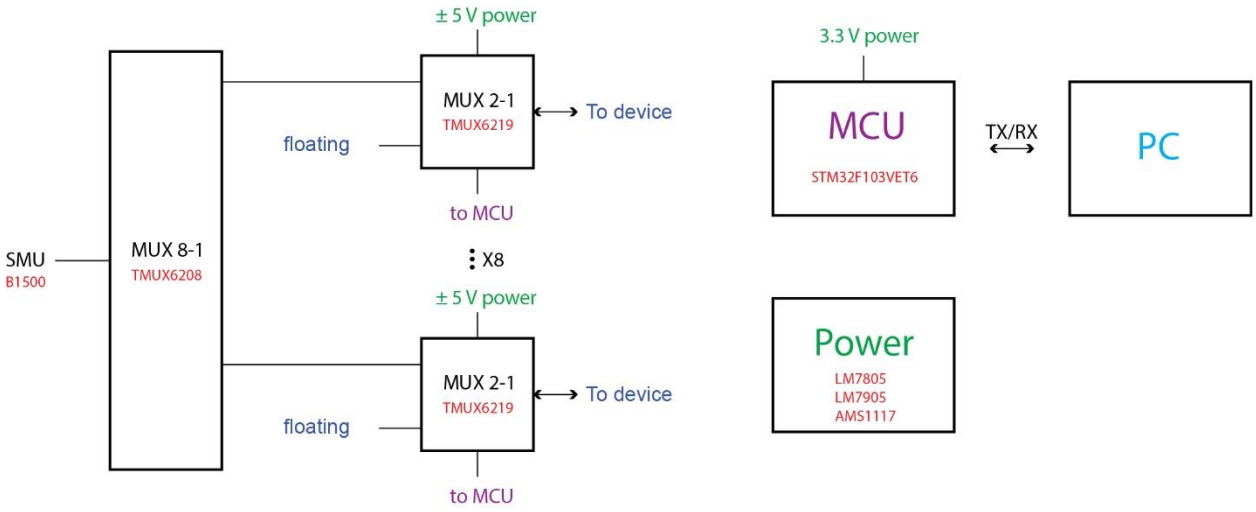
where I_{LRS_min} is the minimal read-out current in the selected cell with a LRS state and I_{HRS_max} is the maximal read-out current in the selected cell with a HRS state. For I_{LRS_min}, the non-MR in the target cell is set to LRS (800 Ω), whereas the rest non-MRs are set to HRS (39.8 kΩ). For I_{HRS_max} , the non-MR in the target cell is set to HRS (39.8 kΩ), whereas the rest non-MRs are set to LRS (800 Ω). Experimental values of the On resistance (~200 Ω) and Off resistance (~300 MΩ) in the BVMR are used. The sampling resistor R_s takes a minimal value (*e.g.*, 1 nΩ) for extracting the total current.

The RMs in arrays with sizes of 4×4, 8×8, 16×16, 32×32, and 64×64 are directly calculated by simulation (LTspice XVII). Values in larger arrays are estimated by extrapolation. Specifically, an error is defined as the difference between the ideal (*i.e.*, RM in a 1×1 array without any sneak-path current) and the actual RMs:

$$Error_{n\times n} = RM_{1\times 1} - RM_{n\times n}\ (n = 4, 8, 16, 32, 64),$$

where $RM_{1\times 1}$ is 97.5% based on above numerical values. We find that $Error_{n\times n}$ has a log-linear trend with n. So a log-linear extrapolation is used to estimate the $Error_{n\times n}$ (for $n > 64$). Then the RM in larger array is estimated by:

$$RM_{n\times n} = RM_{1\times 1} - Error_{n\times n}\ (n > 64)$$



Supplementary Figure S16. Schematic of the peripheral circuit to addressed reading/programming the array. Multiplexers (MUX) were used as the analogue switches to connect selected wordline(WL)/bitline(BL) to a Source Measure Unit (SMU). Specifically, a 8-to-1 multiplexer (MUX 8-1) was used to connect the SMU to eight 2-to-1 multiplexers (MUX 2-1), which were used to select or float the WLs/BLs. The multiplexers were powered by ±5 V power supply, which was achieved by fixed-voltage integrated-circuit voltage regulators (LM7805, LM7905). The multiplexer logic function was controlled by a Microcontroller Unit (MCU, STM32F103VET6), which was powered by a fixed-voltage integrated-circuit voltage regulator (AMS1117). The machine-computer communication was performed by Serial Communication (TX/RX, Transmitter/Receiver).

Supplementary references

1. Fu, T. *et al*. Bioinspired bio-voltage memristors. *Nat. Commun*. **11**, 1861 (2020).
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4. Zhang, L. *et al*. Cell variability impact on the one-selector one-resistor cross-point array performance. *IEEE Trans. Electron Dev.* ***62***, 3490-3497 (2015).