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Letter

Two-Terminal MoS_2 Memristor and the Homogeneous Integration with a MoS_2 Transistor for Neural Networks

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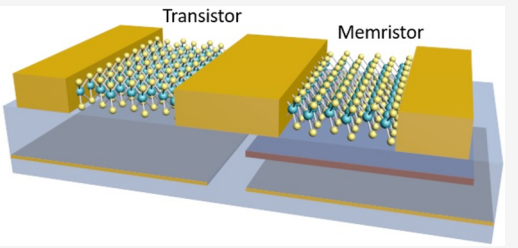
ABSTRACT: Memristors are promising candidates for constructing neural networks. However, their dissimilar working mechanism to that of the addressing transistors can result in a scaling mismatch, which may hinder efficient integration. Here, we demonstrate two-terminal MoS_2 memristors that work with a charge-based mechanism similar to that in transistors, which enables the homogeneous integration with MoS_2 transistors to realize one-transistor−one-memristor addressable cells for assembling programmable networks. The homogenously integrated cells are implemented in a 2 × 2 network array to demonstrate the enabled addressability and programmability. The potential for assembling a scalable network is evaluated in a simulated neural network using obtained realistic device parameters, which achieves over 91% pattern recognition accuracy. This study also reveals a generic mechanism and strategy that can be applied to other semiconducting devices for the engineering and homogeneous integration of memristive systems.



KEYWORDS: *memristor, neural network, MoS_2, 2D materials, transistor*

Memristors have tunable conductance that can emulate the state modulation in neural systems.[1−3] Computing architectures constructed from them can incorporate their state variables to yield in-memory computation, which are considered more efficient than conventional von Neumann systems.[1−4] Although a broad variety of memristors have been discovered and studied, a typical shared challenge in implementing them for scalable integration resides in the stochastic device performance.[2,3] This is attributed to a "destructive" mechanism involved in many devices, in which the atomic structural rearrangement (often at local scale) associated with state change can be dispersive and irreversible,[5,6] resulting in performance nonuniformity across device and time. The filamentary nature in many memristors also suggests that the programming input (*e.g.*, current) does not scale proportionally with device size,[7−10] as opposed to that in the associated addressing device (*e.g.*, transistor) in the architecture. This scaling mismatch presents a challenge for high-density integration, because the addressing device may not be able to shrink accordingly for maintaining the necessary driving current. The problem can be prominent as many existing memristors require a large programming current.[11−13]

The nondestructive charge-based mechanism in transistors ensures the reliability and scalability, making them a mature technology.[14] Constructing a memristive device from transistor structures can therefore harness these benefits to improve integration. Charge injection in the floating gate is often employed to tune the channel conduction for modulable states. These floating-gate transistors have been used to construct programmable computing systems, including programmable digital logics demonstrated first with semiconductor nanowires,[15,16] and then two-dimensional (2D) materials.[17] Analog neural networks have also been proposed based on floating-gate transistors.[18] However, state modulation through a third gate terminal deviates from the simplicity offered by the two-terminal configuration in typical memristors, which is deemed advantageous for constructing a computing network.

The feasibility of constructing a two-terminal, charge-based memristor from transistor structure was suggested from a two-terminal nonvolatile memory device made from a semiconducting carbon nanotube.[19] It was demonstrated that the drain voltage, in addition to producing an in-plane field for conduction, also yielded an out-of-plane field that pumped charge into the dielectric layer to modulate the channel conduction. The effect was also observed in graphene, although the modulation was not as large due to its lack of a bandgap.[20] Later developments employed 2D materials with inherent bandgap to yield a large On/Off ratio for constructing two-terminal nonvolatile memories.[21] However, all of these studies focused on the digital state modulation in the devices. Analog conductance modulation was only recently demon-

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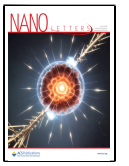

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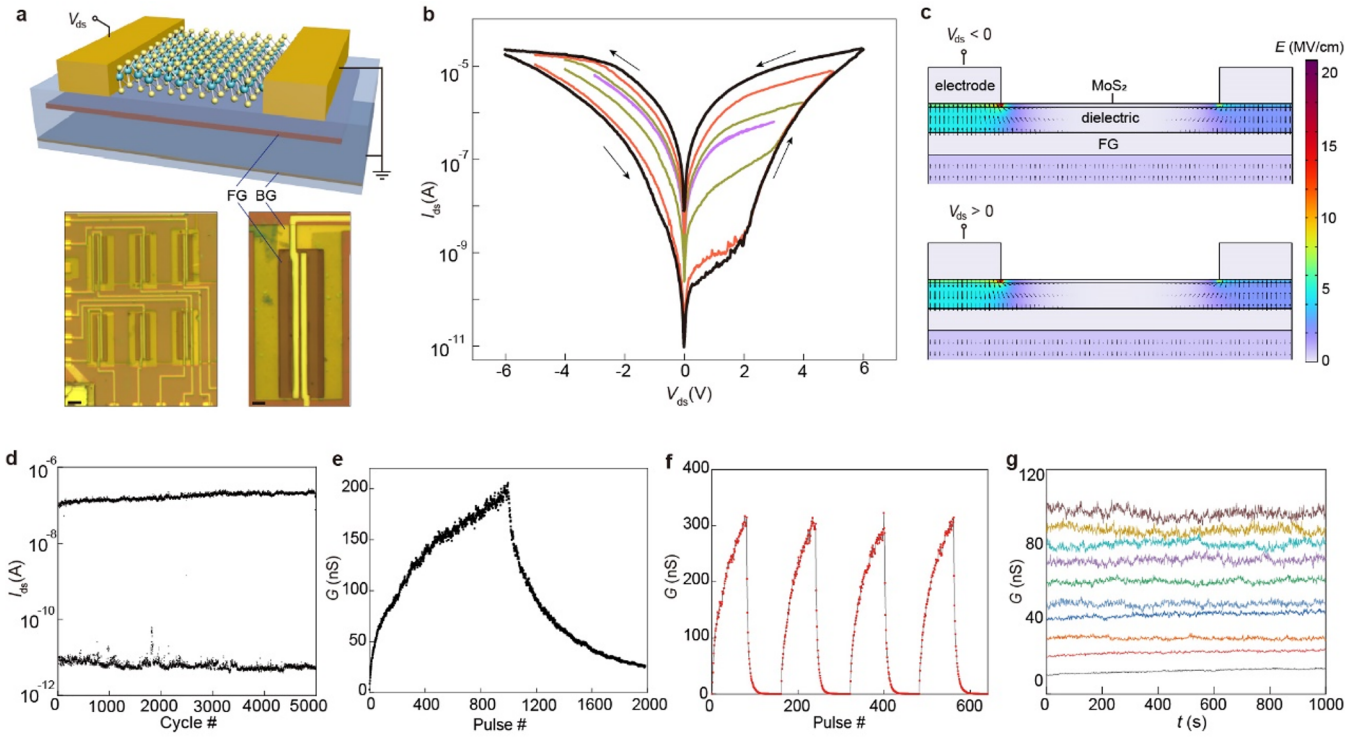

Figure 1. Two-terminal memristive effect in the MoS_2 device. **a**, (Top) Schematic of the MoS_2 device structure, in which a floating gate (FG) is defined underneath the MoS_2 channel and a back gate (BG) serving as the global reference is grounded. The bottom panel shows optical images of the fabricated MoS_2 device array (left) and an individual device (right). Scale bars, 20 μm (left) and 5 μm (right). **b**, A series of two-terminal $I-V$ sweeps in a MoS_2 device, showing drain voltage (V_{ds})-dependent hysteresis. **c**, Simulated electric field distribution in the MoS_2 device with $V_{ds} = -6$ V (top) and $V_{ds} = 6$ V (bottom). Note that here a 60-nm channel length was used for better display. The simulation showed that the field distribution at the drain region was very close between a 60-nm channel and a 1-μm channel. **d**, Programming cycles in the MoS_2 device. A $\pm$7 V pulse (5 s) was applied to the drain to program the On/Off state and a -0.1 V was used to read the conductance in each cycle. **e**, Analog conductance modulation by continuously applying 1000 Set pulses (3 V, 60 ms) and 1000 Reset pulses (-6 V, 60 ms) at the drain. The conductance was read out after each programming pulse by -0.1 V. **f**, Repeated analog programming cycles. Each cycle involved 80 Set pulses (3.5 V, 60 ms) and 80 Reset pulses (-6.5 V, 60 ms), with the conductance read out by -0.1 V right after each programming pulse. **g**, Retention in 10 programmed states continuously monitored with -0.1 V.

strated in a two-terminal MoS_2 transistor structure by using exfoliated graphene and boron nitride as the charge trapping and tunneling layers, respectively, with the demonstration limited to a single device for emulating synaptic behavior.[22]

Here, we demonstrate two-terminal charge-based MoS_2 memristors and the homogeneous integration with MoS_2 transistors to realize one-transistor–one-memristor (1T1R) addressable cells for assembling a programmable network. The synaptic weight in the MoS_2 memristor can be modulated with four-bit precision against the noise level, while the MoS_2 transistor enables selective addressing and programming of the memristor. The 1T1R cells are implemented in a 2 × 2 crossbar array to demonstrate the enabled programmability. The potential for assembling a scalable network is evaluated in a simulated neural network using obtained realistic device parameters, which achieves a pattern recognition rate of >91%.

We first studied the two-terminal memristive effect in an individual MoS_2 transistor structure, which was fabricated from polycrystalline monolayer MoS_2 synthesized by the metal–organic chemical vapor deposition (MOCVD) method as described previously[23] (Figure 1a). The MoS_2 layer was contacted by a pair of source and drain electrodes with a channel length of 1 μm and a width of 50 μm. A 5 nm Au layer, separated by a 7 nm Al_2O_3 tunneling layer,[24,25] was defined underneath to serve as the charge-trapping layer. A bottom gate, further beneath the trapping layer and separated by a 30 nm Al_2O_3 insulating layer, was defined as the global reference (*e.g.*, ground).

For the two-terminal measurement, a drain voltage (V_{ds}) was applied with both the source and global reference grounded. In a series of current–voltage ($I-V$) sweeps (black curves, Figure 1b), the device changed from a high-resistance state (HRS) to a low-resistance state (LRS) during a forward voltage sweep (0 → 6 V). The device maintained the LRS during the backward voltage sweep (6 → 0 V), showing nonvolatile state modulation. The voltage sweeps in the negative region (0 → −6; −6 → 0 V) showed an opposite trend, with the device changing from an LRS to an HRS. Together, these $I-V$ characteristics featured typical memristor behavior.

We performed the following investigations to reveal the charge-based origin of the memristive effect. First, a single-crystalline MoS_2 flake was also used to fabricate a device of the same structure, which showed $I-V$ curves with a similar memristive effect (see Supporting Information Figure S1). The result excluded the possibility of the memristive effect being caused by grain-boundary-mediated migration of defects in the polycrystalline MoS_2.[26,27] Second, the field distribution in the device structure was simulated, which revealed a large vertical component (~ 4.6 MV/cm) at the drain injection boundary (Figure 1c). This vertical field component is sufficient for charge injection through the tunneling layer.[28] Specifically, a negative drain voltage creates an upward field that attracts

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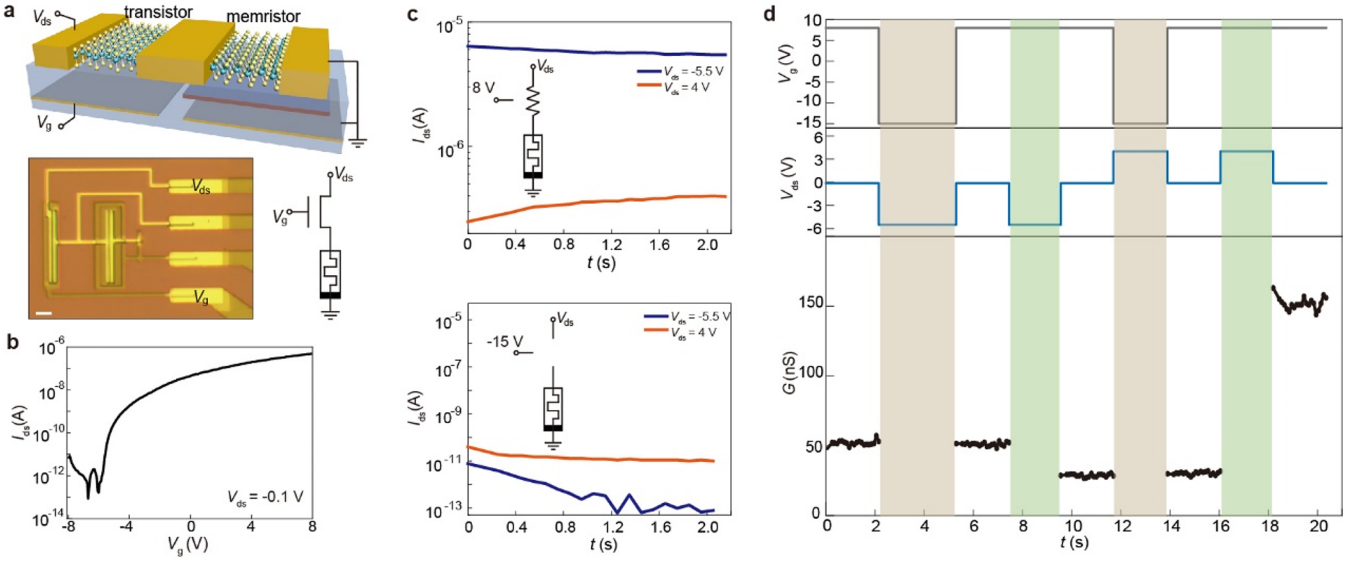

Figure 2. Homogeneous integration. **a**, (Top) Schematic of the homogeneous 1T1R cell integrated from a MoS_2 transistor and a MoS_2 memristor, with the corresponding circuit diagram (bottom right) and the optical image of a fabricated cell (bottom left). Scale bar, 20 μm. Note that in the fabricated cell, an addressing electrode was added between the transistor and memristor for the convenience of testing each device separately. **b**, A representative transport curve in the MoS_2 transistor, showing typical *n*-type behavior. **c**, (Top) In a selected cell (transistor On, represented by an equivalent resistor in the inset), the current gradually increased (orange) and decreased (blue) with applied V_{ds} of 4 V and −5.5 V, respectively. (Bottom) In the deselected cell (transistor Off, represented by an open circuit in the inset), the current remained negligible with applied V_{ds}. The insets show the corresponding equivalent circuits. **d**, Demonstration of selective Set and Reset programming in the cell.

electrons to the trapping layer (upper panel, Figure 1c), which is expected to produce an effective negative gate effect and reduce the conduction in the *n*-type MoS_2 channel to produce a Reset process. Conversely, a positive drain voltage creates a downward field that depletes the electron in the trapping layer (bottom panel, Figure 1c), which is expected to increase the channel conduction to produce a Set process. These expectations were consistent with experimental observations (Figure 1b). Reducing the amplitude of V_{ds} led to a decrease in the vertical field component (Supporting Information Figure S2), which is expected to reduce the memristive effect. This was again consistent with the experimental results, in which the $I-V$ hysteresis became less prominent with a decrease in the amplitude of V_{ds} (color curves, Figure 1b). Third, this generic mechanism of drain-induced charge injection was further supported by two-terminal devices fabricated from other semiconducting nanomaterials such as Si and Ge/Si nanowires[15,16,29,30] which demonstrated a similar memristive effect (see Supporting Information Figure S3). The MoS_2-based device showed a lower switching voltage than those of these nanowire-based devices, possibly because the 2D flat MoS_2−substrate interface has better charge injection efficiency compared to the 1D nanowire−substrate contact.

Similar to other memristors, the conductance state in the MoS_2 device can be modulated by pulsed programming (*i.e.*, V_{ds} pulse). In a series of Set-and-Reset cycles (Figure 1d), the device showed distinct LRS and HRS. A confined distribution was observed in both the LRS and HRS, consistent with the expectation from a nondestructive charge-based mechanism that can reduce dispersity in device performance. Controlling the amount of charge injection into the trapping layer through the number of V_{ds} pulses led to the continuous modulation of the conductance states in the device (Figure 1e). The linearity in the modulation was comparable to or better than previous MoS_2 memristors based on ion/defect migrations[26,27,31,32] (see Supporting Information Figure S4). This analog modulation was reversible and repeatable (Figure 1f), with the programmed states maintaining a stable value over time (Figure 1g). These results suggested that the device can function as a synaptic weight in a neural network. Note that the noise (Figure 1g) was revealed to have the $1/f$ origin (see Supporting Information Figure S5), which increases with the increase of conductance.[33] Nevertheless, the relative noise level remained within the range of 2%, which did not significantly affect the emulated neural function, as will be discussed later. The noise is expected to be suppressed by reducing surface contaminants or interfacial defects.[33]

The programming current in many filamentary memristors does not scale with device size,[7−10] preventing a proportionate scaling in the addressing device (*e.g.*, transistor). The charge-based mechanism in the memristor provides an opportunity for proportionate scaling between the memristor and addressing transistor, enabling effective integration. Importantly, homogeneous integration by constructing both devices from the same material can further improve parameter matching and ease fabrication. Thus, we studied the feasibility of constructing both device elements in the 1T1R programmable cell from the same MoS_2 material. Specifically, we adopted similar structural parameters for addressing the MoS_2 transistor and MoS_2 memristor due to material homogeneity (Figure 2a). The constructed MoS_2 transistor showed typical *n*-type behavior in the current-and-gate ($I_{ds}-V_g$) transport curve, featuring an On/Off ratio > 10^5 (Figure 2b) convenient for selector function.[34] For selective programming in the 1T1R cell, the transistor is first turned On (*e.g.*, with V_g = +8 V) and then a Reset/Set voltage is applied to its drain. This drain voltage is expected to largely drop across the MoS_2 memristor if its programmable resistance range is chosen to be much larger than the resistance of the MoS_2 transistor. Experimentally, an applied drain voltage of +4 V yielded a gradual current increase

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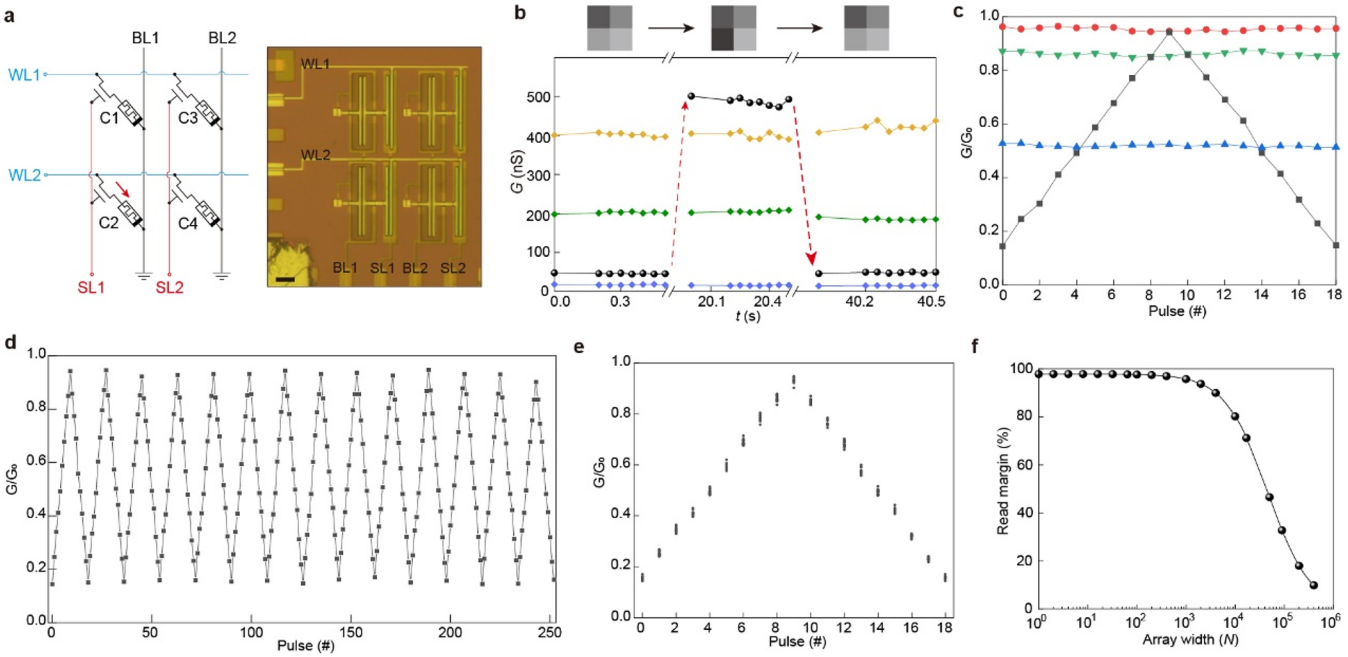

Figure 3. 2 × 2 array integration. **a**, (Left) Circuit diagram of 1T1R-based 2 × 2 addressable array. (Right) Optical image of a fabricated 2 × 2 array constructed from MoS_2 1T1R cells. Scale bar, 20 μm. **b**, Selective programming of cell 2 (C2) in the array from the conductance of 50 nS to 500 nS and then back to 50 nS (black curves), with the conductance in the rest cells unchanged (color curves). **c**, The conductance in the selected C2 cell (black dots) was set to 10 increasing levels and then reset to 10 decreasing levels (between 70−480 nS). The increasing levels were programmed a series of Set (4 V) pulses of 0.2, 0.4, 0.4, 0.8, 1, 1.2, 1.8, 1.8, and 1.8 s, respectively. The decreasing levels were programmed by a series of Reset (−5.3 V) pulses of 0.1, 0.1, 0.2, 0.4, 0.6, 1, 2.6, 4.4, and 8.6 s, respectively. Due to the tunneling nature (*e.g.*, injection current has exponential increase with the voltage), much faster programming is possible by using larger voltages.[22] The conductance in the rest of the cells was unchanged (color dots) during the process. **d**, Repeated programming in the same cell using the same parameters in (c). **e**, The distribution in each of the 10 conductance levels during the repeated programming in (d). **f**, Simulated read margin with respect to the array width (N) based on performance parameters in the MoS_2 memristor and transistor (1 μm channel length and 50 μm channel width).

in the cell (orange, top panel; Figure 2c), suggesting successful continuous Set programming in the MoS_2 memristor. Conversely, an applied drain voltage of −5.5 V yielded a gradual current decrease in the cell (blue, top panel, Figure 2c), suggesting a successful continuous Reset programming in the MoS_2 memristor. Deselecting the cell by tuning Off the MoS_2 transistor (e.g., V_g = −15 V) yielded negligible current with applied Set/Reset voltage (bottom panel, Figure 2c), suggesting successful suppression of both the current and voltage drop across the MoS_2 memristor to prevent its state change.

The controlled programmability in the 1T1R cell was further demonstrated in a series of pulse programming. As shown in Figure 2d, the initial conductance state of ∼50 nS (t = 0−2.2 s, bottom panel) in the memristor was retrieved by turning on the transistor (V_g = +8 V, top panel) and applying a read voltage of −0.1 V at the drain (middle panel). If the cell was deselected by turning off the MoS_2 transistor (V_g = −15 V), an applied Reset voltage of −5.5 V at the drain (t = 2.2−5.3 s) did not alter the state in the memristor (t = 5.3−7.5 s). If the cell was selected by turning on the transistor (V_g = +8 V), then a Reset voltage of −5.5 V applied at the drain (t = 7.5−9.6 s) reduced the conductance in the memristor to ∼30 nS (t = 9.6−11.7 s). Similarly, if the cell was unselected, then an applied Set voltage of 4 V (t = 11.7−13.9 s) could not alter the memristor state (t = 13.9−16.1 s). If the cell was selected, then the same applied Set voltage (t = 16.1−18.2 s) increased the conductance in the memristor to ∼150 nS (t = 18.2−20.4 s). These results show that the MoS_2-based homogeneous 1T1R structure can serve as an addressable cell for the construction of a programmable network.

We then implemented the cells in a cross-bar array to evaluate the selective programmability for network applications. Since the sneak paths in a crossbar array are essentially composed of 2 × 2 paths,[35] we studied the feasibility in a 2 × 2 array without losing generality (Figure 3a). The array shared the same structure as the existing 1T1R memristor network,[34] in which the shared drain input in the row, shared source input in the column, and shared gate control of the transistors (selectors) served as the word line (WL), bit line (BL), and selection line (SL), respectively. For selective programming/reading (*e.g.*, in cell C2), a gate voltage (+8 V) is applied to SL1 to turn on the selectors along the line, and a gate voltage (−15 V) is applied to the remaining SL2 to turn off the selectors along the line. A programming/reading voltage is applied to WL2 with WL1 floating. For the selected cell C2, the operation is expected to be the same as demonstrated in the individual cell (Figure 2). The WL2 input is expected to have no effect on C4 since it is deselected, whereas the floating input from WL1 also ensures that C1 and C3 are not programmed/read. The 1T1R addressing scheme described above can be extended to larger array sizes, ensuring that all nontarget cells are either deselected or unbiased. This is different from a neural network constructed using the three-terminal flash memory architecture,[36] in which the Reset programming involves erasing the entire column and rewriting all other cells in that column.

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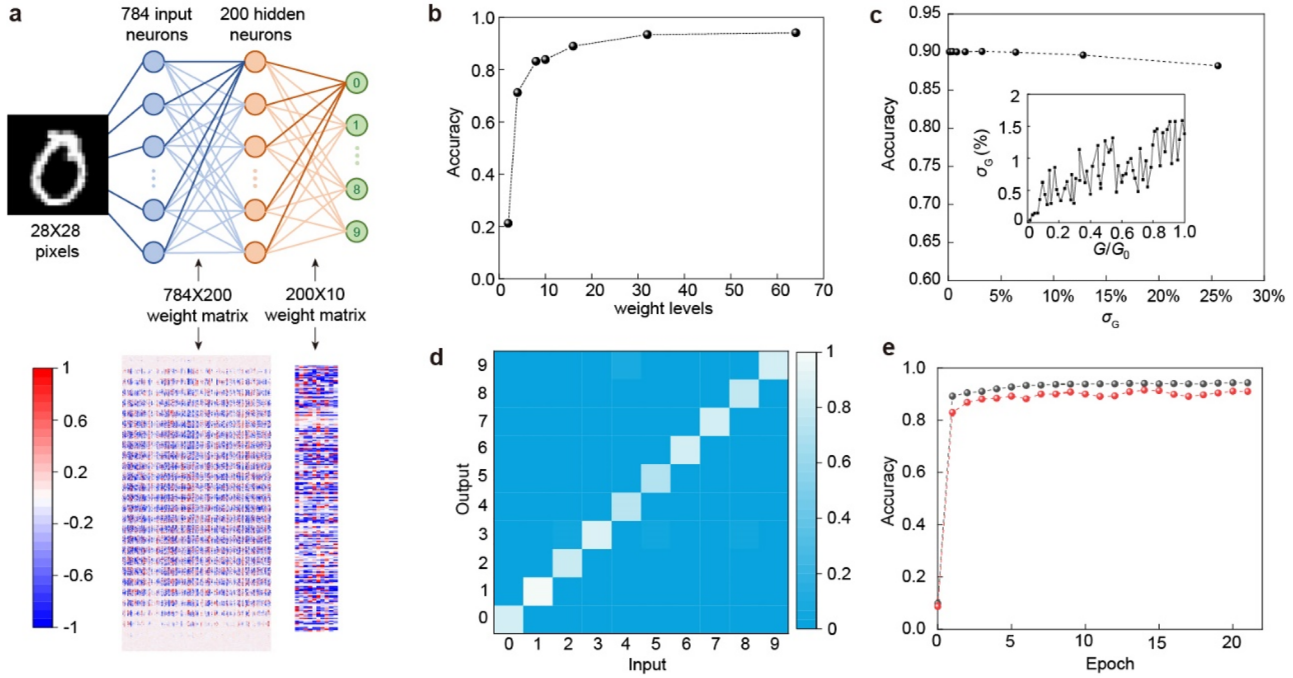

Figure 4. Simulated neural network based on MoS_2 1T1R cells. **a**, (Top) Structure of a 3-layer neural network for digit recognition, with the weight matrices constructed from two 1T1R crossbar arrays. The bottom panel shows an exemplary set of (4-bit) weight matrices from a trained network. **b**, Recognition rate or accuracy with respect to the available states (weight levels) in each cell in the simulated network. **c**, Recognition accuracy with respect to added noise in the network with 4-bit weight precision (*i.e.*, 16 available states in each cell). The inset shows the actual measured noise σ_G (defined as the standard deviation of the relative conductance fluctuation)[38] in 64 programmed states from a MoS_2 memristor. **d**, Recognition accuracy for each digit using the network of 4-bit weight precision and 1.5% added noise. **e**, Comparison of the recognition accuracy between a realistic network of 4-bit weight precision and 1.5% added noise (red dots) and an ideal one with arbitrary weight precision and no noise (black dots).

The testing results were consistent with the above analysis. The conductance of the selected C2 cell was changed from ~ 50 nS to ~ 500 nS (black curve, Figure 3b) by applying Set programming pulses of + 4 V to WL2 with SL1 selected (+8 V). The conductance states in the remaining cells (color curves) remained unchanged during the process. Similarly, the conductance of the selected C2 cell was changed from ~500 to ~50 nS by applying Reset programming pulses of −5.5 V to WL2 with SL1 selected (+8 V), without altering the states in the remaining cells. These results demonstrate the addressable and reversible programmability that is key to the weight update in a neural network. Furthermore, the conductance state in the selected cell can be continuously modulated by the number and width of programming pulses to control the cumulative charge injection in the trapping layer. A 10-state reversible programming in the selected C2 cell was readily achieved with the control of Set/Reset pulses (black curve, Figure 3c). The states in the unselected cells remained unchanged throughout the process (color curves). The state modulation in the selected cell was repeatable (Figure 3d), with each of the programmed states highly converged (Figure 3e). These results show the reliability of the addressing strategy for selective and continuous weight update. Smaller updates with more state levels are possible by using a reduced pulse width (Figure 1e). The selective programming in the 2 × 2 array validates that the homogeneous 1T1R MoS_2 cells can be implemented in scalable arrays for programmable networks. The excellent selection ratio in the MoS_2 transistor suggests that the width (N) in an $N \times N$ array can be scaled to $>10^5$ to maintain a read margin > 20% (Figure 3f; see detailed analysis in Supporting Information Figure S6).

We therefore evaluated the potential of implementing the 1T1R cells in a network for a realistic task (*e.g.*, handwritten digit recognition) based on the revealed device performance. Handwritten digits were obtained from the modified National Institute of Standards and Technology (MNIST) database and were normalized within a 28 × 28 pixel bounding box. A three-layer neural network was employed for the task, consisting of a layer of 784 input neurons (*e.g.*, corresponding to the 28 × 28 input pixel number), a layer of 200 hidden neurons, and a layer of 10 output neurons (top, Figure 4a; see detailed procedure in Supporting Information Figure S7). The synaptic weight matrices were constructed from simulated arrays of 784 × 200 and 200 × 10 MoS_2 1T1R cells (bottom, Figure 4a). A set of 5000 randomly selected images from the MNIST database was used for training[37] (e.g., an epoch), and a set of 1000 randomly selected images was used for recognition testing.

The weight precision (*i.e.*, state levels in the cell) is expected to affect the recognition accuracy. Our simulation showed that the accuracy increased with the increase of the number of available weight levels in the cell. An accuracy > 90% was achieved with 16-level or four-bit state modulation in the cell (Figure 4b), which was readily attainable in the MoS_2 memristor (Figure 1e). To get a close representation of a realistic situation, noise in the weight was further added. The noise[38] in 64 programmed weight levels from the MoS_2 memristor was measured, showing a dominant distribution within 1.5% (inset, Figure 4c). Noise was randomly added to the 16-state network. The network showed robustness again noise, with a recognition accuracy > 88% maintained at a noise level of 25% (Figure 4c). The accuracy increased to > 90% within the noise level of 1.5%, which covered the dominant

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noise levels in the MoS_2 memristor (inset). Specifically, the network with a 4-bit weight precision and 1.5% noise, corresponding to realistic MoS_2 device performance, showed consistent accuracy for the individual recognition of the 10 digits (Figure 4d). The overall accuracy was only ~3% lower compared with an ideal network that had arbitrary weight precision without noise (Figure 4e). These results show the potential of implementing MoS_2 1T1R cells in realistic neural networks.

The recent development of ultralow contact resistance in MoS_2 devices has expanded the potential for device scaling.[39] The shared transport mechanism and electronic parameters in the MoS_2 transistor and memristor suggest that they can be proportionately scaled in the homogeneous 1T1R integration if an effective selection (*e.g.*, On/Off ratio) in the transistor and charge trapping in the memristor are retained. To demonstrate the potential, we fabricated a 1T1R cell in which both the memristor and transistor were reduced to a size of $1 \times 0.2\ \mu m^2$. Both devices maintained good performance, enabling selective programming in the 1T1R cell (Supporting Information Figure S8). Furthermore, recent experimental and simulation studies have shown that both transistor performance and charge-trapping memory effect are retained even when the MoS_2 channel length is reduced to below 50 nm.[18,40,41] These studies indicate that the effective size of the homogeneously integrated 1T1R MoS_2 cell can be scaled down to sub-100 nm size, which is smaller than existing heterogeneous 1T1R cells with sizes beyond the micrometer scale due to mismatched scaling.[12,42] Meanwhile, the Off resistance in the transistor/selector determines the sneak-path current level, which also means that its ratio to the upper-bound resistance in the MoS_2 memristor will affect the scalability.[35] Taking these values from sub-50 nm MoS_2 transistors in a previous study,[41] our estimate shows that the width (N) in an integrated $N \times N$ array can be over 10^4 (see Supporting Information Figure S9), which is larger than existing ones and sufficient for various functions. Improving the MoS_2 material quality and device engineering, which are of common interest in the field, is expected to improve the potential of 1T1R integration. The two-terminal MoS_2 memristors also enable the feasibility of integration with two-terminal selectors,[34] including homogeneous MoS_2-based selectors,[43] for a simplified crossbar architecture.

Our study also suggests a generic mechanism that can be applied to other semiconducting materials to engineer two-terminal charge-based memristors and enable homogeneous 1T1R integration. This approach has the potential to create a broad category of neuromorphic systems. It is likely that this strategy can be applied to silicon technology for expedited development because it offers the maturity and well-controlled interface that are crucial for ensuring reliability and uniformity at a large scale for array integration.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.2c05007.

Figures S1−S9 describing additional single-crystalline device performance, field simulation, nanowire device performance, linearity analysis, noise analysis, read margin calculation, neural network emulation, device scaling, and read margin simulation, respectively (PDF)

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Author Contributions

J.Y. and S.F. conceived the project and designed experiments. S.F. carried out experimental studies in device and circuit fabrication and measurement. J.H.P. synthesized the polycrystalline MoS_2. T.Z. and J.X. synthesized the single-crystalline MoS_2. J.K. oversaw the 2D material production. H.G. helped with the fabrication of nanowire devices. T.F. helped with the simulation. L.S. helped with electrical measurement. J.Y. and S.F. wrote the manuscript. All authors discussed the results and implications and commented on the manuscript.

Notes

The authors declare no competing financial interest.

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